Principal Design Engineer

Essential Duties:

- Responsible for development of state-of-the-art design for low power wireless SoCs
- Work with verification team to collaborate on test plan, coverage plan, and coverage closure; additionally, helping with design verification when needed
- Experience with low power design & verification techniques with UPF/CPF is a plus
- Work with physical design team on design constraint and timing closure
- Work with systems team during design bring up on Silicon or FPGA/Palladium platform
- Work with cross-functional teams and coordinate priorities to achieve higher productivity

Qualifications:

- BSEE or MSEE with 10+ years of experience in designing complex IP, SoC with RF integrated, or mixed-signal ASIC products
- ASIC Macro/Micro architecture Design, Verilog RTL Coding, low power design, and SoC chip level clock/reset structure design
- Experience with front-end design flow and corresponding tools.
- Experience with Lint, Synthesis, Equivalence Checking, Static Timing Analysis and DFT
- Familiarity with Verilog Simulation/Verification (Conventional – both RTL and gate level, Assertion Based, Formal)
- Design Debug and Validation
- Design Documentation
- Knowledge of ARM CPU, AXI, and memory controllers is needed
- Excellent analytical and problem solving skills
- Excellent oral and written communication skills
- Proven teamwork skills. Prior experience in startup environment, working in small team setup a plus